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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/832,892	04/12/2001	Takehisa Yamaguchi	205975US2	1675

22850 7590 06/02/2003

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER

NGUYEN, HOAN C

ART UNIT	PAPER NUMBER
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2871

DATE MAILED: 06/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/832,892

Applicant(s)

YAMAGUCHI ET AL.

Examiner

HOAN C. NGUYEN

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on 3/25/03.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) 6-13 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

Applicant's arguments with respect to Amended claims 1-13 have been considered but are moot in view of the new ground(s) of rejection. **Therefore, this is Final action.**

Election/Restrictions

Applicant's election with traverse of Group I (claims 1-5) in Paper No. 4 is acknowledged.

Applicant's arguments regarding the restriction requirement have been considered; however, the traversal was on the grounds that there is no serious burden on the Examiner in examining all of claims 1-13 together. This is not found persuasive since Takaski discloses the different method of making display with source electrode 103 and two drain electrodes 102 being formed directly on substrate. However, the invention disclose source and drain electrodes formed on the gate insulating film.

Therefore, the requirement is deemed proper.

Claims 6-13 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected inventions and species, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-3 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Takashi (JP1267617).

Takashi teaches (Fig. 1) a liquid crystal display comprising:

- a gate electrode line 106 including a gate electrode formed on an insulating substrate;
- a source electrode line 108 including a source electrode 103 intersected with said gate electrode line 106 via an insulating film (gate insulating film 105);
- a thin film transistor including said gate electrode, said source electrode, and two drain electrodes located in a vicinity of a portion in which said gate electrode line is intersected with said source electrode line;
- two drain electrode lines 102, each including a portion acting as one of the two drain electrodes, said two drain electrode lines being connected with a pixel electrode 107;

wherein

- said two drain electrodes are located on opposite sides of said source electrode with each of said two drain electrodes having a near side opposed to said source electrode that is superposed with said gate electrode and a far side opposed to near side that is not superposed with said gate electrode.
- an area of a region where said gate electrode line 106 is superposed with the near side of one of said two drain electrodes is substantially identical to an area

of a region where said gate electrode is superposed with the other one of said two drain electrodes as shown in Fig. 1b according to claim 2.

- a length of a region in a channel lengthwise direction of said thin film transistor where said gate electrode is superposed with the near side of one of said two drain electrodes is substantially identical to a length 109 of a region in a channel lengthwise direction of said thin film transistor where said gate electrode line is superposed with the near side of other one of said two drain electrodes according to claim 3,
- said two drain electrodes are formed in whole part of one end of said drain electrode line in a channel widthwise direction where the near side of each drain electrode is superposed with said gate electrode line according to claim 5;

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takashi (JP1267617) as applied to claims 1-3 above.

It is conventional in the thin film transistor manufacture that said length of the region in the channel lengthwise direction is such a length as to prevent current characteristics from degradation in a thin film transistor.

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Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display with the thin film transistor manufacture that said length of the region in the channel lengthwise direction is such a length for preventing current characteristics from degradation in a thin film transistor.

Response to Arguments

Applicant's arguments filed on 3/25/2003 have been fully considered but they are not persuasive.

Applicant's ONLY arguments are follows:

Takaski fails to disclose drain electrodes having the near sides thereof facing a source electrode superimposed over a gate electrode with the far sides of each drain electrode opposed to the near side not being superimposed over the gate electrode.

Examiner's responses to Applicants' ONLY arguments are follows:

Takaski discloses drain electrodes having the near sides thereof facing a source electrode superimposed over a gate electrode with the far sides of each drain electrode opposed to the near side not being superimposed over the gate electrode and being connected to pixel electrode (see attachment).

Conclusion


Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAN C. NGUYEN whose telephone number is (703) 306-0472. The examiner can normally be reached on MONDAY-THURSDAY:8:00AM-4:30PM. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0530.

HOAN C. NGUYEN
Examiner
Art Unit 2871

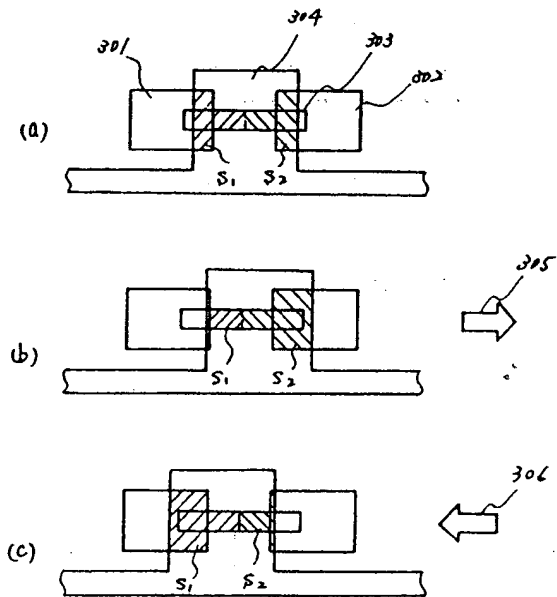
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May 28, 2003


SUPERVISOR
EXAMINER
2003

代理人 井理士 上 柳 雅 誓 (他 1 名)

Figure 1 is a schematic diagram of a semiconductor device. The top part is a plan view (A) showing a substrate 107 with a central region 104. A vertical line B-B' passes through the center. A horizontal line 103 is shown on the left. A vertical line 102 is shown on the right. A horizontal line 108 is shown at the top. A horizontal line 109 is shown below 103. A horizontal line 106 is shown below 109. A horizontal line 110 is shown below 106. The bottom part is a cross-sectional view showing a substrate 101. A layer 102 is on top of 101. A layer 104 is on top of 102. A layer 105 is on top of 104. A layer 106 is on top of 105. A layer 107 is on top of 106. A layer 108 is on top of 107. A layer 109 is on top of 108. A layer 110 is on top of 109. The labels 101, 102, 104, 105, 106, 107, 108, 109, 110 are used to identify the various layers and components.

第 1 図



第 3 図

第 2 図